**Amendments to the Claims:**

1. (original) A method of generating soft bit outputs from soft symbol decisions for an *M*-ary symbol alphabet in a communication receiver coupled to a channel wherein said communication receiver includes a first decoder adapted to generate said soft symbol decisions from a received signal, said method comprising the steps of:

receiving *M* soft symbol decisions for each symbol, wherein each symbol is represented by *m* bits;

partitioning said soft symbol decisions into *m* bit groups, each said bit group comprising a zero-bit portion and a one-bit portion;

summing all soft symbol values in the zero-bit portion of a particular bit group of interest, so as to generate a first sum;

summing all soft symbol values in the one-bit portion of a particular bit group of interest, so as to generate a second sum;

computing a soft bit value for the particular bit of interest as a function of said first sum and said second sum; and

wherein *m* and *M* are positive integers.

2. (original) The method according to claim 1, wherein said communications receiver is adapted to receive and decode a global system for mobile communication (GSM) signal.

3. (original) The method according to claim 1, wherein said communications receiver is adapted to receive and decode a GSM EDGE Radio Access Network (GERAN) system signal.

4. (original) The method according to claim 1, further comprising the step of providing a second decoder operative to generate receive binary data in accordance with said soft bit output values.

5. (original) The method according to claim 4, wherein said second decoder comprises a convolutional decoder based on the Viterbi Algorithm (VA).

6. (original) The method according to claim 1, wherein said *M*-ary symbol comprises an 8-PSK symbol.

7. (original) The method according to claim 1, wherein said step of computing comprises generating said soft bit values represented as bit log likelihood ratios (LLRs).

8. (original) The method according to claim 1, wherein said soft symbol values are represented as symbol log likelihood ratios (LLRs).

9. (original) The method according to claim 1, wherein said zero-bit portion comprises those soft symbol decisions that correspond to those symbols having a zero bit in the particular bit position of interest.

10. (original) The method according to claim 1, wherein said one-bit portion comprises those soft symbol decisions that correspond to those symbols having a one bit in the particular bit position of interest.

11. (original) The method according to claim 1, wherein said first decoder comprises a maximum likelihood sequence estimation (MLSE) equalizer based on the Soft Output Viterbi Algorithm (SOVA).

12. (original) The method according to claim 1, wherein said first decoder comprises means for performing maximum a posterior (MAP) algorithm.

13. (original) The method according to claim 1, wherein said soft bit values are generated in accordance with the function given by

$$LLR(b_j) = \ln\left(\sum_{l \in D_{j1}} e^{LLR(s_k = A_l)}\right) - \ln\left(\sum_{l \in D_{j0}} e^{LLR(s_k = A_l)}\right)$$

wherein LLR($s_k$=$A_l$) is the log likelihood ratio of symbol $s_k$=$A_l$, $A_l$ represents the symbol value, $b_j$ represents the $j^{th}$ bit of the symbol, $D_{j0}$ and $D_{j1}$ represent the set of symbols wherein bit $j$ = 0 and 1, respectively, $\forall l \in D_{ji}$ and $b_j(A_l)$=$i$ for $i$=0, 1; $j$=0,..., $m$-1; $l$=0,..., $M$-1.

14. (original) The method according to claim 13, further comprising the step of outputting said soft bit values to a soft second decoder for decoding into binary data therefrom.

15. (original) The method according to claim 1, further comprising the step of outputting said soft bit values to a de-interleaver whose output is subsequently input to a soft second decoder for decoding into binary data therefrom.

16. (original) The method according to claim 1, wherein said $M$ soft symbol decisions for each symbol comprise $M$-1 soft symbol decisions and an implied reference symbol.

17. (original) The method according to claim 1, wherein said step of computing comprises computing a Max-Log approximation with a refinement.

18. (previously amended) A method of generating soft bit outputs from soft symbol values for an $M$-ary symbol alphabet, said method comprising the steps of:

receiving for each symbol $m$+1 soft symbol values represented as symbol log likelihood ratios wherein each symbol is represented by $m$ bits, and wherein said $m$+1 soft symbol values comprise a first soft symbol value corresponding to a most likely symbol and $m$ second soft symbol values, wherein each said second soft symbol value corresponds to a symbol closest in Euclidean distance to said most likely symbol whose bit in the position of interest is opposite that of the analogous bit in said most likely symbol;

computing a soft bit value for each bit of interest as a function of said first soft symbol value and said $m$ second soft symbol values; and

wherein $m$ and $M$ are positive integers.

19. (original) The method according to claim 18, wherein said $M$-ary symbols are transmitted in a global system for mobile communication (GSM) network.

20. (previously amended) The method according to claim 18, wherein said method of generating soft bit outputs is implemented in a GSM EDGE Radio Access Network (GERAN) system.

21. (original) The method according to claim 18, further comprising the step of providing an outer decoder operative to generate receive binary data in accordance with said soft bit outputs.

22. (original) The method according to claim 21, wherein said outer decoder comprises a convolutional decoder based on the Viterbi Algorithm (VA).

23. (original) The method according to claim 18, wherein said *M*-ary symbol comprises an 8-PSK symbol.

24. (original) The method according to claim 18, wherein said step of computing comprises generating said soft bit values represented as bit log likelihood ratios (LLRs).

25. (canceled)

26. (original) The method according to claim 18, wherein said soft symbol decisions are generated by a maximum likelihood sequence estimation (MLSE) equalizer based on the Soft Output Viterbi Algorithm (SOVA).

27. (original) The method according to claim 18, wherein said soft symbol decisions are generated by a maximum a posterior (MAP) algorithm based equalizer.

28. (original) The method according to claim 18, wherein said soft bit values are generated from the $m+1$ soft symbol values whereby the most likely log likelihood value is compared with one other symbol log likelihood value corresponding to a bit value opposite to that of the bit of interest.

29. (original) The method according to claim 28, further comprising the step of outputting said soft bit values to a soft decoder for decoding into binary data therefrom.

30. (original) The method according to claim 18, further comprising the step of outputting said soft bit values to a de-interleaver whose output is subsequently input to a soft decoder for decoding into binary data therefrom.

31. (original) The method according to claim 18, wherein said step of computing comprises computing a Max-Log approximation with a refinement.

32. (original) A method of generating soft bit outputs from soft symbol decisions for an *M*-ary symbol, said method comprising the steps of:

receiving $M$ soft symbol decisions for each symbol, wherein each symbol is represented by $m$ bits;

partitioning said soft symbol decisions into *m* bit groups, each said bit group comprising a zero-bit portion and a one-bit portion;

selecting, for each bit group of interest, a first maximum soft symbol value from among the soft symbol values in said zero-bit portion;

selecting, for each bit group of interest, a second maximum soft symbol value from among the soft symbol values in said one-bit portion;

computing a soft bit value for each bit of interest as a function of said first maximum soft symbol value and said second maximum soft symbol value; and

wherein *m* and *M* are positive integers.

33. (original) The method according to claim 32, wherein said *M*-ary symbols are transmitted in a global system for mobile communication (GSM) network.

34. (previously amended) The method according to claim 32, wherein said method of generating soft bit outputs is implemented in a GSM EDGE Radio Access Network (GERAN) system.

35. (original) The method according to claim 32, further comprising the step of providing an outer decoder operative to generate receive binary data in accordance with said soft bit output values.

36. (previously amended) The method according to claim 35, wherein said outer decoder comprises a convolutional decoder based on the Viterbi Algorithm (VA).

37. (original) The method according to claim 32, wherein said *M*-ary symbol comprises an 8-PSK symbol.

38. (original) The method according to claim 32, wherein said step of computing comprises generating said soft bit values represented as bit log likelihood ratios (LLRs).

39. (original) The method according to claim 32, wherein said soft symbol values are represented as symbol log likelihood ratios (LLRs).

40. (original) The method according to claim 32, wherein said zero-bit portion comprises those soft symbol decisions that correspond to those symbols having a zero bit in the particular bit position of interest.

41. (original) The method according to claim 32, wherein said one-bit portion comprises those soft symbol decisions that correspond to those symbols having a one bit in the particular bit position of interest.

42. (original) The method according to claim 32, wherein said soft symbol decisions are generated by a maximum likelihood sequence estimation (MLSE) equalizer based on the Soft Output Viterbi Algorithm (SOVA).

43. (original) The method according to claim 32, wherein said soft symbol decisions are generated by a maximum a posterior (MAP) algorithm based equalizer.

44. (currently amended) The method according to claim 32, wherein said soft bit values are generated from said soft symbol values whereby [[the]] a most likely log likelihood value is compared with one other symbol log likelihood value corresponding to a bit value opposite to that of the bit of interest.

45. (original) The method according to claim 44, further comprising the step of outputting said soft bit values to a soft decoder for decoding into binary data therefrom.

46. (original) The method according to claim 32, wherein said step of computing comprises computing a Max-Log approximation with a refinement.

47. (previously amended) The method according to claim 32, further comprising the step of outputting said soft bit values to a de-interleaver whose output is subsequently input to a soft outer decoder for decoding into binary data therefrom.

48. (original) The method according to claim 32, wherein said $M$ soft symbol decisions for each symbol comprise $M$-1 soft symbol decisions and an implied reference symbol.

49. (currently amended) A method of generating soft bit ~~outputs~~ information from soft symbol ~~values~~ information, said method comprising the steps of:

~~receiving for each symbol a plurality of soft symbol values represented as symbol log likelihood ratios;~~

~~determining, for each bit in said symbol, a first likelihood representing the probability that said bit is a one, said first likelihood determined based on said symbol log likelihood ratios;~~

~~determining, for each bit in said symbol, a second likelihood representing the probability that said bit is a zero, said second likelihood determined based on said symbol log likelihood ratios; and~~

~~computing a soft bit value for said bit as a function of said first likelihood and said second likelihood.~~

receiving a plurality of soft symbol values for each symbol;

determining, for each bit position of interest, a first soft symbol value corresponding to a maximum soft symbol value wherein the bit of interest is a zero and a second soft symbol value corresponding to a maximum soft symbol value wherein a bit of interest is a one;

utilizing an overall maximum soft symbol value for either said zero bit or said one bit in accordance with the value of the bit in the bit position of interest of said overall maximum soft symbol;

utilizing for the other bit, the value of a soft symbol closest in Euclidean distance to said overall maximum soft symbol whose bit in the position of interest is opposite that of the analogous bit in said overall maximum soft symbol; and

approximating a log likelihood ratio for a particular bit of interest as the difference between said second soft symbol value and said first soft symbol value.

50. (currently amended) The method according to claim 49, ~~wherein said first likelihood is determined by summing the soft symbol values for all symbols wherein said bit is a one~~ wherein said soft symbol values are represented as log likelihood ratios.

51. (currently amended) The method according to claim 49, ~~wherein said second likelihood is determined by summing the soft symbol values for all symbols wherein said bit is a zero~~ wherein said soft symbol information is provided for an 8-PSK symbol.

52. (currently amended) The method according to claim 49, ~~wherein said first likelihood comprises the maximum soft symbol value from among all symbol values wherein said bit is a~~

~~one~~ wherein said soft symbol values are generated by a maximum a posteriori (MAP) algorithm based equalizer.

53. (currently amended) The method according to claim 49, ~~wherein said second likelihood comprises the maximum soft symbol value from among all symbol values wherein said bit is a zero~~ further comprising the step of outputting said soft bit information to a soft decoder for decoding into binary data therefrom.

54. (currently amended) A communications receiver for receiving and decoding an *M*-ary transmitted signal, comprising:

a radio frequency (RF) front end circuit for receiving and converting said *M*-ary transmitted signal to a baseband signal;

a demodulator adapted to receive said baseband signal and to generate a received signal therefrom in accordance with the *M*-ary modulation scheme used to generate said transmitted signal;

a first decoder operative to receive said received signal and to generate a sequence of soft symbol decisions therefrom;

a soft symbol ~~decision~~ to soft bit output converter comprising processing means programmed to:

~~receive for each symbol a plurality of soft symbol values represented as symbol log likelihood ratios;~~

~~determine, for each bit in said symbol, a first likelihood representing the probability that said bit is a one, said first likelihood determined based on said symbol log likelihood ratios;~~

~~determine, for each bit in said symbol, a second likelihood representing the probability that said bit is a zero, said second likelihood determined based on said symbol log likelihood ratios;~~

~~compute a soft bit value for said bit as a function of said first likelihood and said second likelihood; and~~

receive a plurality of soft symbol values for each symbol;

determine, for each bit position of interest, a first soft symbol value corresponding to a maximum soft symbol value wherein the bit of interest is a zero and a

second soft symbol value corresponding to a maximum soft symbol value wherein a bit of interest is a one;

utilize an overall maximum soft symbol value for either said zero bit or said one bit in accordance with the value of the bit in the bit position of interest of said overall maximum soft symbol;

utilize for the other bit, the value of a soft symbol closest in Euclidean distance to said overall maximum soft symbol whose bit in the position of interest is opposite that of the analogous bit in said overall maximum soft symbol;

approximate a log likelihood ratio for a particular bit of interest as the difference between said second soft symbol value and said first soft symbol value; and

a second decoder adapted to receive said soft bit values and to generate binary received data therefrom.

55. (previously amended) The receiver according to claim 54, further comprising a speech decoder operative to convert the output of said second decoder to an audible speech signal.

56. (previously amended) The receiver according to claim 54, further comprising circuit switch data means for converting the output of said second decoder to a data stream.

57. (previously amended) The receiver according to claim 54, further comprising packet switch data means for converting the output of said second decoder to a data stream.

58. (original) The receiver according to claim 54, wherein said communications receiver is adapted to receive and decode a Global System for Mobile Communication (GSM) signal.

59. (currently amended) The ~~method~~ receiver according to claim 54, wherein said communications receiver is adapted to receive and decode a GSM EDGE Radio Access Network (GERAN) system signal.

60. (original) The receiver according to claim 54, wherein said second decoder comprises a convolutional decoder based on the Viterbi Algorithm (VA).

61. (original) The receiver according to claim 54, wherein said *M*-ary symbol comprises an 8-PSK symbol.

62. (currently amended) The receiver according to claim 54, further comprising the step of generating said soft decision ~~value~~ values represented as [[a]] log likelihood ~~ratio~~ ratios (LLR).

63. (original) The receiver according to claim 54, wherein said first decoder comprises a maximum likelihood sequence estimation (MLSE) equalizer based on the Soft Output Viterbi Algorithm (SOVA).

64. (original) The receiver according to claim 54, wherein said first decoder comprises means for performing maximum a posterior (MAP) algorithm.

65. (currently amended) The receiver according to claim 54, wherein said soft bit values are computed from said soft symbol values whereby [[the]] a most likely log likelihood value is compared with one other symbol log likelihood value corresponding to a bit value opposite to that of the bit of interest.

66. (currently amended) The ~~method~~ receiver according to claim 54, wherein said step of ~~computing~~ approximating comprises computing a Max-Log approximation with a refinement.

67. (original) The receiver according to claim 54, further comprising the step of outputting said soft bit values to a de-interleaver whose output is subsequently input to a soft second decoder for decoding into binary data therefrom.

68. (currently amended) [[An]] The receiver according to claim 54, wherein said processing means comprises an electronic data storage media storing a computer program adapted to ~~program a computer to execute the soft output generator process of claim 54~~ execute on said processing means for implementing said soft symbol to soft bit converter.

69. (currently amended) A computer readable storage medium having a computer program embodied thereon for causing a suitably programmed system to generate soft output values by performing the following steps when such program is executed on said system:

~~receiving for each symbol a plurality of soft symbol values represented as symbol log likelihood ratios;~~

~~determining, for each bit in said symbol, a first likelihood representing the probability that said bit is a one, said first likelihood determined based on said symbol log likelihood ratios;~~

~~determining, for each bit in said symbol, a second likelihood representing the probability that said bit is a zero, said second likelihood determined based on said symbol log likelihood ratios; and~~

~~computing a soft bit value for said bit as a function of said first likelihood and said second likelihood.~~

receiving a plurality of soft symbol values for each symbol;

determining, for each bit position of interest, a first soft symbol value corresponding to a maximum soft symbol value wherein the bit of interest is a zero and a second soft symbol value corresponding to a maximum soft symbol value wherein a bit of interest is a one;

utilizing an overall maximum soft symbol value for either said zero bit or said one bit in accordance with the value of the bit in the bit position of interest of said overall maximum soft symbol;

utilizing for the other bit, the value of a soft symbol closest in Euclidean distance to said overall maximum soft symbol whose bit in the position of interest is opposite that of the analogous bit in said overall maximum soft symbol; and

approximating a log likelihood ratio for a particular bit of interest as the difference between said second soft symbol value and said first soft symbol value.

70. (currently amended) The computer readable storage medium according to claim 69, wherein said computer program is suitably programmed to ~~determine said first likelihood by summing the soft symbol values for all symbols wherein said bit is a one~~ represent soft symbol values as log likelihood ratios.

71. (currently amended) The computer readable storage medium according to claim 69, wherein said computer program is suitably programmed to ~~determine said second likelihood by summing the soft symbol values for all symbols wherein said bit is a zero~~ provide soft symbol information for an 8-PSK symbol.

72. (currently amended) The computer readable storage medium according to claim 69, wherein said computer program is suitably programmed to ~~obtain said first likelihood by determining the maximum soft symbol value from among all symbol values wherein said bit is a one~~ generate soft symbol values by a maximum a posteriori (MAP) algorithm based equalizer.

73. (currently amended) The computer readable storage medium according to claim 69, wherein said computer program is suitably programmed to ~~obtain second likelihood by determining the maximum soft symbol value from among all symbol values wherein said bit is a zero~~ output said soft bit information to a soft decoder for decoding into binary data therefrom.

74. (currently amended) The computer readable storage medium according to claim 69, wherein said step of ~~computing~~ approximating comprises computing a Max-Log approximation with a refinement.